0CE77 95TT260

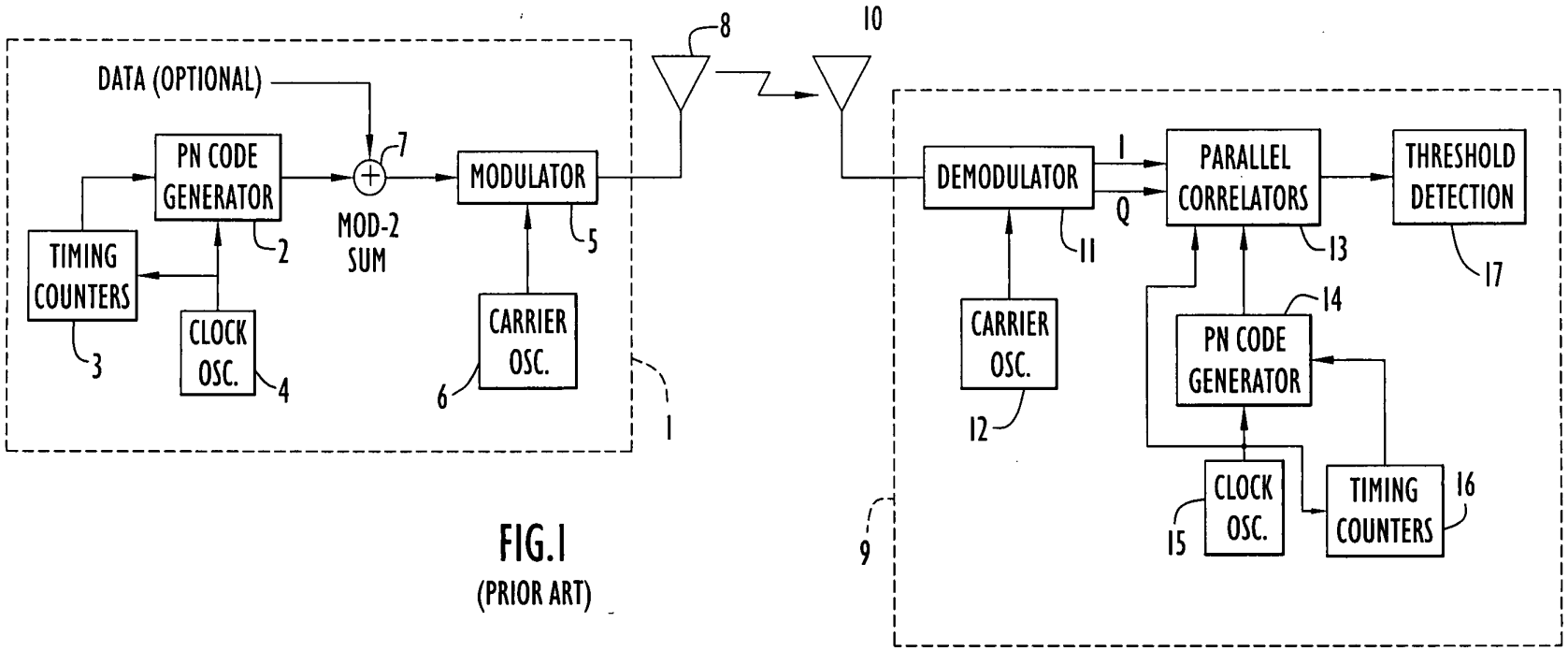


FIG.1
(PRIOR ART)

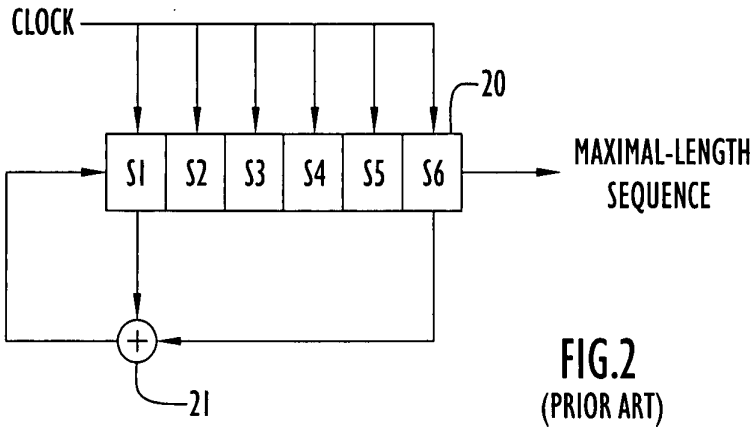


FIG.2
(PRIOR ART)

FIG.3A

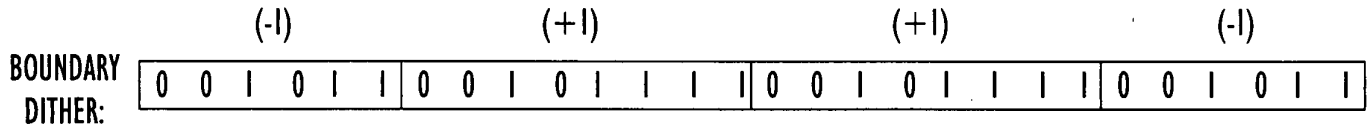


FIG.3B

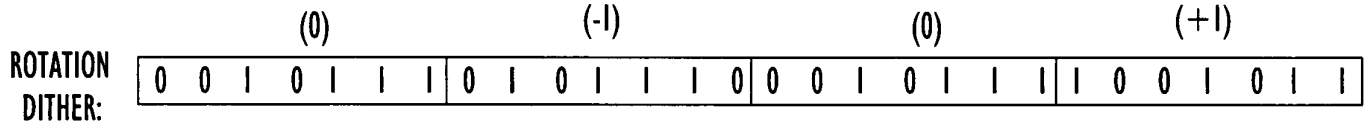
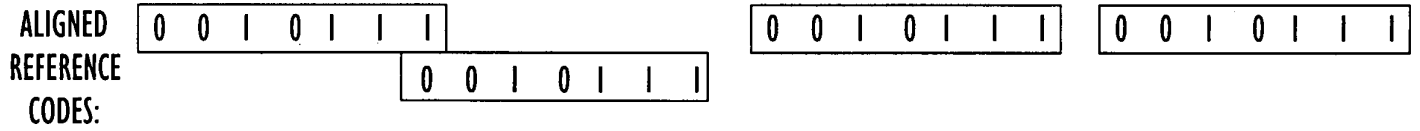


FIG.3C



DOCKET 95TT260

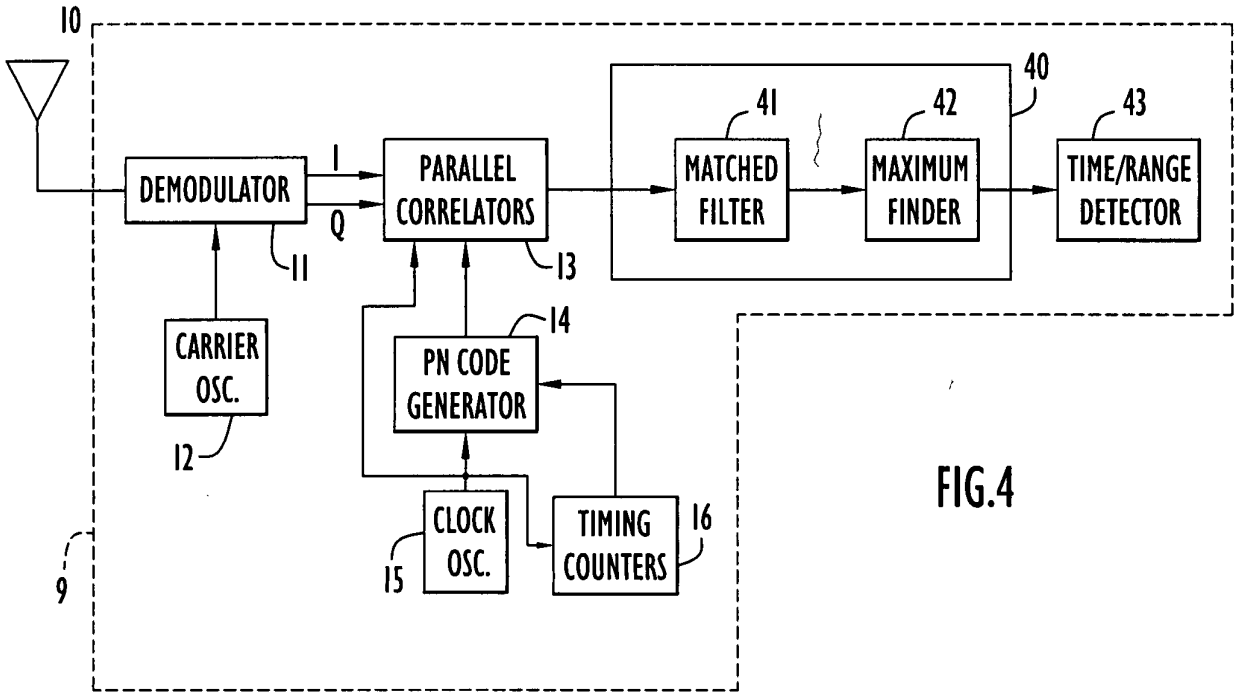


FIG.4

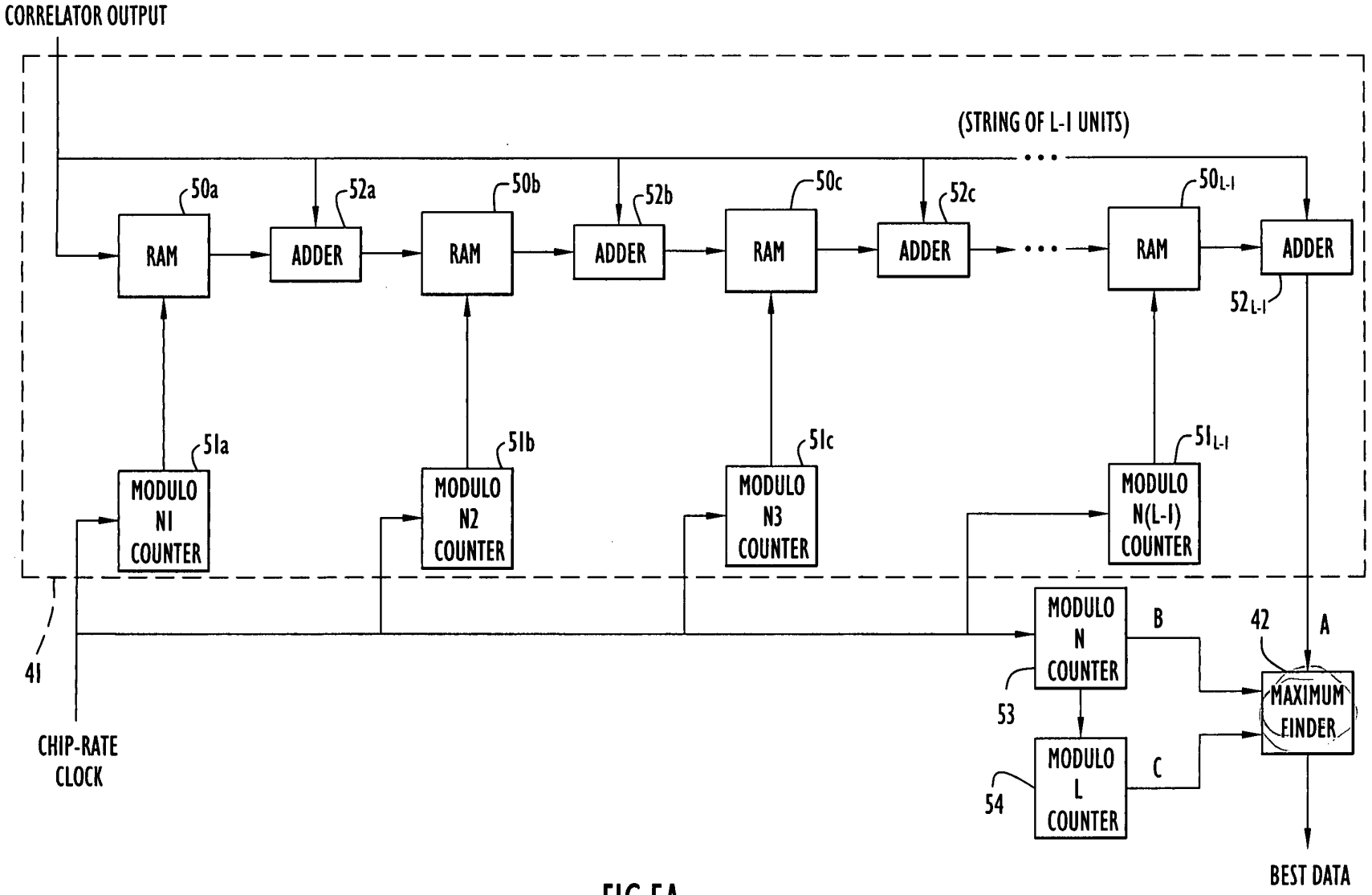

CORRELATOR OUTPUT
(STRING OF L-1 UNITS)
50a
52a
50b
52b
50c
52c
50L-1
RAM
ADDER
RAM
ADDER
RAM
ADDER
RAM
ADDER
52L-1
51a
51b
51c
51L-1
MODULO N1 COUNTER
MODULO N2 COUNTER
MODULO N3 COUNTER
MODULO N(L-1) COUNTER
41
CHIP-RATE CLOCK
MODULO N COUNTER
B
42
A
53
MAXIMUM FINDER
MODULO L COUNTER
54
C
BEST DATA

FIG.5A

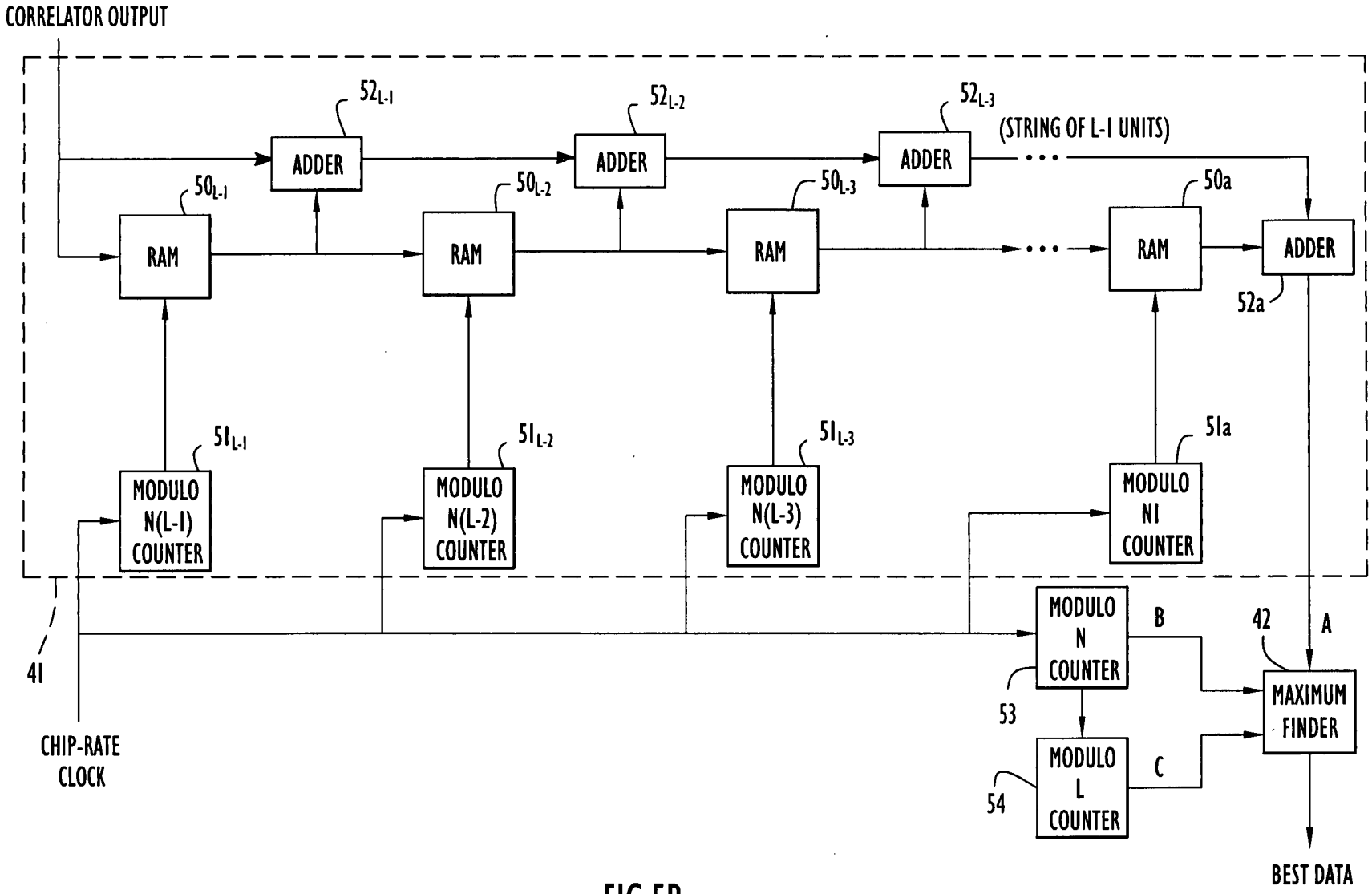

CORRELATOR OUTPUT
ADDER
ADDER
ADDER
(STRING OF L-1 UNITS)
ADDER
RAM
RAM
RAM
RAM
MODULO N(L-1) COUNTER
MODULO N(L-2) COUNTER
MODULO N(L-3) COUNTER
MODULO N1 COUNTER
MODULO N COUNTER
MODULO L COUNTER
MAXIMUM FINDER
CHIP-RATE CLOCK
BEST DATA
A
B
C
41
42
53
54
50a
52a
51a

FIG.5B

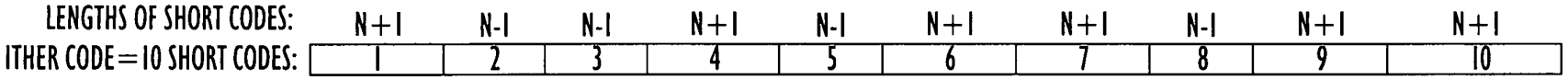


FIG.6A

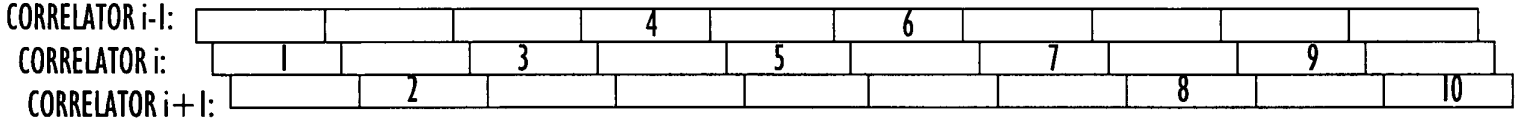


FIG.6B

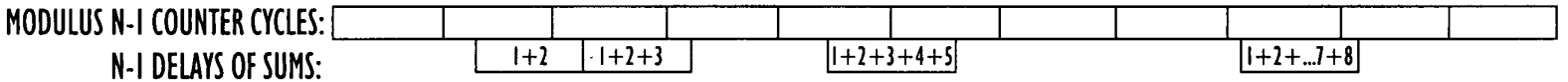


FIG.6C

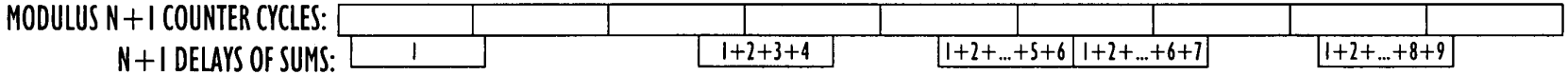


FIG.6D

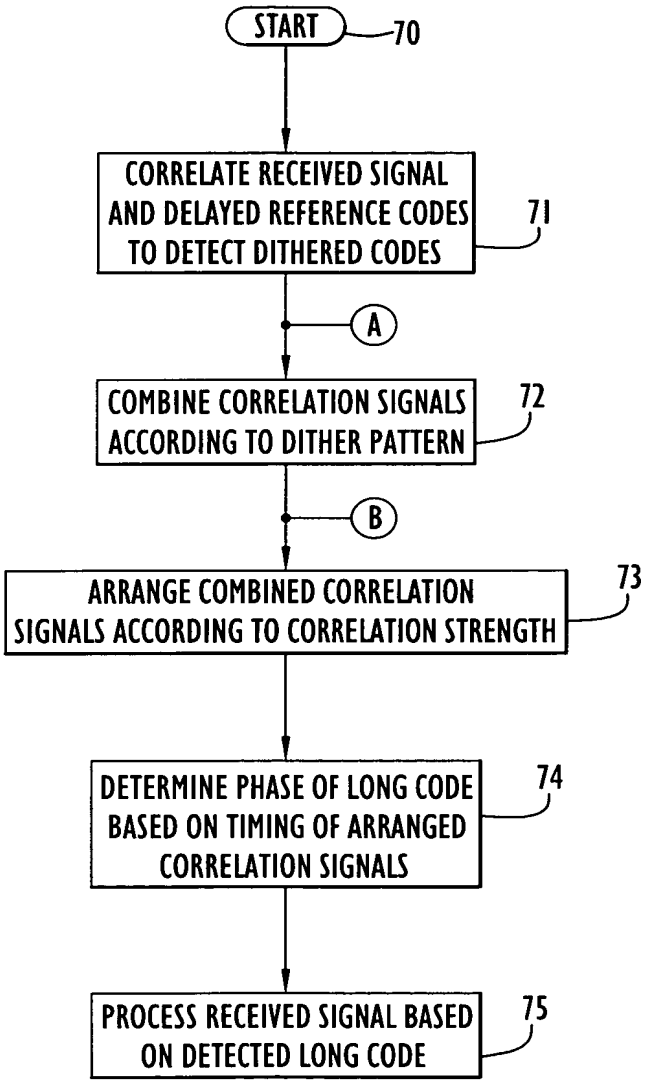

START
70
CORRELATE RECEIVED SIGNAL AND DELAYED REFERENCE CODES TO DETECT DITHERED CODES
71
A
COMBINE CORRELATION SIGNALS ACCORDING TO DITHER PATTERN
72
B
ARRANGE COMBINED CORRELATION SIGNALS ACCORDING TO CORRELATION STRENGTH
73
DETERMINE PHASE OF LONG CODE BASED ON TIMING OF ARRANGED CORRELATION SIGNALS
74
PROCESS RECEIVED SIGNAL BASED ON DETECTED LONG CODE
75

FIG.7A

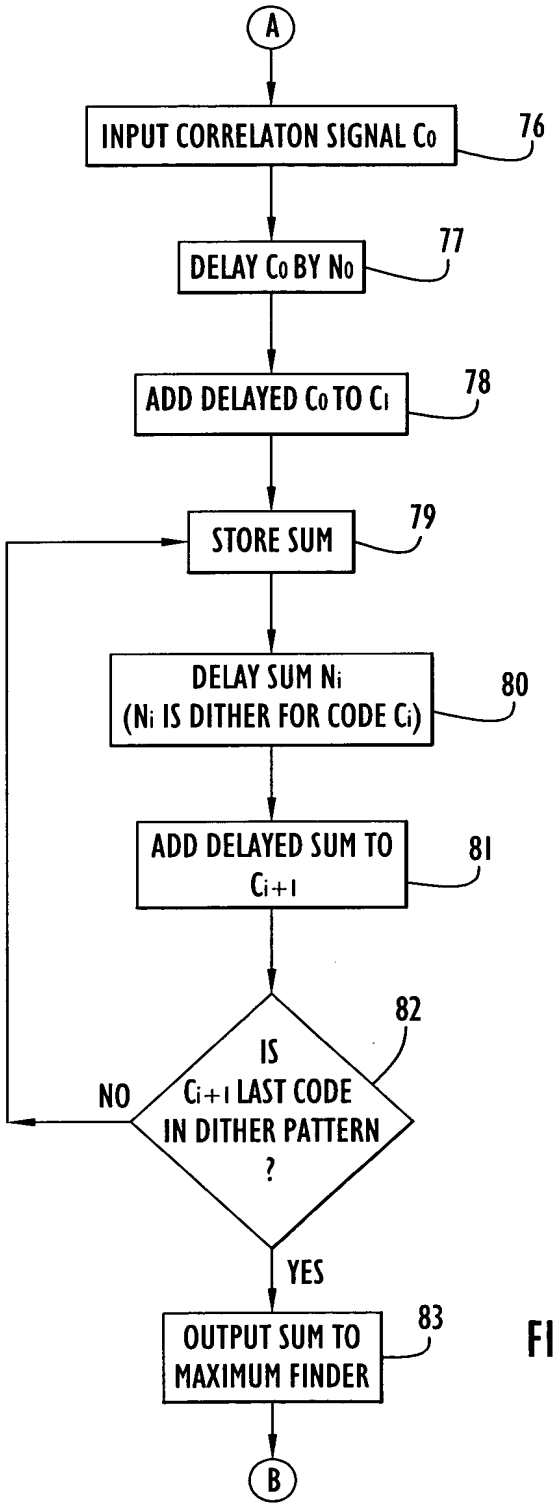

A
INPUT CORRELATON SIGNAL Co
76
DELAY Co BY No
77
ADD DELAYED Co TO Ci
78
STORE SUM
79
DELAY SUM Ni
(Ni IS DITHER FOR CODE Ci)
80
ADD DELAYED SUM TO
Ci+1
81
IS
Ci+1 LAST CODE
IN DITHER PATTERN
?
82
NO
YES
OUTPUT SUM TO
MAXIMUM FINDER
83
B

FIG.7B

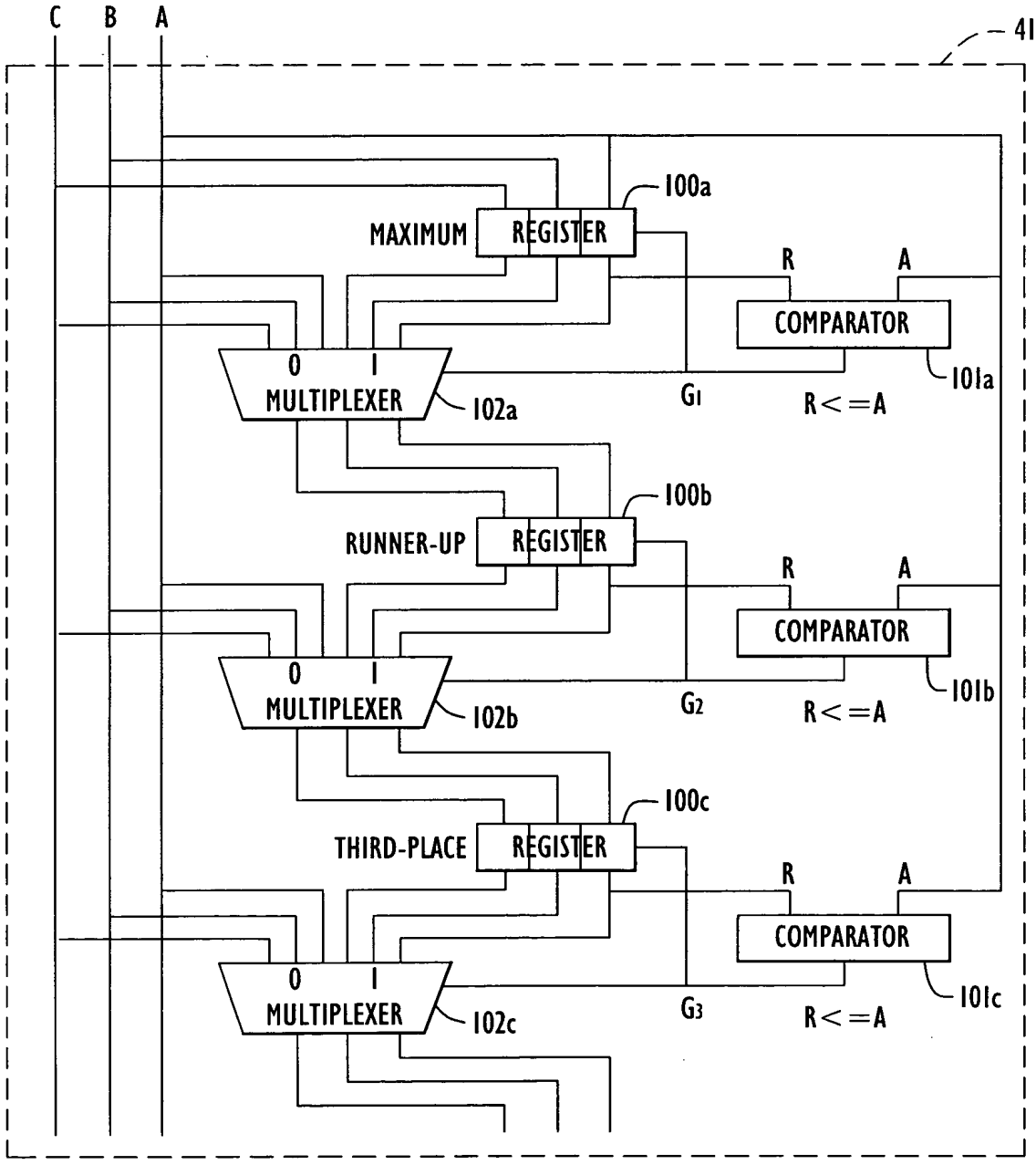

C
B
A
41
100a
MAXIMUM
REGISTER
R
A
COMPARATOR
101a
0
1
MULTIPLEXER
102a
G1
R<=A
100b
RUNNER-UP
REGISTER
R
A
COMPARATOR
101b
0
1
MULTIPLEXER
102b
G2
R<=A
100c
THIRD-PLACE
REGISTER
R
A
COMPARATOR
101c
0
1
MULTIPLEXER
102c
G3
R<=A

FIG.8

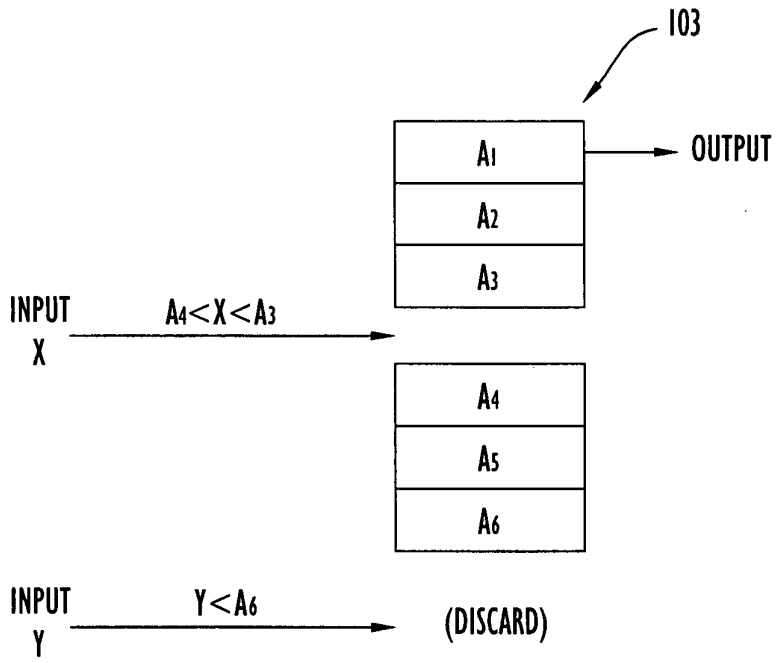


FIG.9